# EXP:16

# DESIGN AND IMPLEMENTATION OF 3-BIT SYNCHRONOUS UP/DOWN COUNTER

AIM:

To design and implement a 3-bit synchronous up/down counter using JK flip-flops and

to verify the count sequence.

EQUIPMENTS & COMPONENTS REQUIRED:

|  |  |  |
| --- | --- | --- |
| Sl. No. | Equipments & Components | Quantity |
| 1 | Digital IC Trainer Kit | 1 |
| 2 | ICs 7476, 7404, 7411, 7486, 7432, 7408 | 2, 1, 1, 1, 1, 1 respectively |
| 3 | Connecting wires | As Required |

THEORY:

Synchronous counters are different from the ripple counters in that the clock pulses are applied to the input of all flip-flops. A common clock pulse triggers all flip-flops. It has an up/down control input with which it counts up or down. If the control input value = 1, the counter counts up and counts down for control input value = 0.

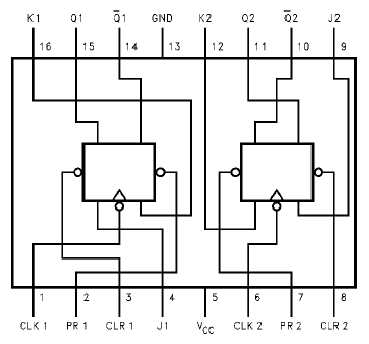
IC 7476 consists of two JK flip-flops with PRESET & CLEAR. The pin diagram is as shown in figure.

PROCEDURE:

1. Test all the ICs manually/ using IC tester.
2. Connect VCC and the ground.
3. Connect the appropriate pins to the input and output LEDs and switches.
4. Verify the truth table with respect to the clock.

PIN DIAGRAM, TRUTH TABLE & LOGIC DIAGRAM:

PIN DIAGRAM FOR IC 7476:



FUNCTION TABLE FOR IC 7476:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | | | Outputs | |
| Preset | Clear | Clock | J | K | Q | Q’ |
| 0 | 1 | x | x | x | 1 | 0 |
| 1 | 0 | x | x | x | 0 | 1 |
| 0 | 0 | x | x | x | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | No Change | No Change |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | Toggle | Toggle |

*Synchronous 3-bit Up/Down Counter:*

COUNT SEQUENCE:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| UD | Present Sate | | | Next State | | | Flip-flop inputs | | | | | |
| Q2 | Q1 | Q0 | Q2 | Q1 | Q0 | J2 | K2 | J1 | K1 | J0 | K0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | x | 1 | x | 1 | x |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | x | 0 | x | 0 | x | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | x | 0 | x | 1 | 1 | x |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | x | 0 | 0 | x | x | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | x | 1 | 1 | x | 1 | x |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | x | x | 0 | x | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | x | x | 1 | 1 | x |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | x | 0 | x | x | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | x | 0 | x | 1 | x |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | x | 1 | x | x | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | x | x | 0 | 1 | x |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | x | x | 1 | x | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | x | 0 | 0 | x | 1 | x |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | x | 0 | 1 | x | x | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | x | 0 | x | 0 | 1 | x |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | x | 1 | x | 1 | x | 1 |

*K-maps for Excess-3 code output bits:*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 |  |  | x | | | x |
| x |  | x | x | | | x |
|  | |
| x | | x |  | | | x |
|  | x |  |
|  | |  |  | 1 |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | x |  | x | x | | | x |
|  | 1 |  |  |  | | |  |
|  | | |
|  | | |  |  | 1 |  |  |
| x | | | x |  | x |  | x |
|  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| (UD)Q2\Q1Q0 | 00 |  | 01 |  | 11 |  | 10 |
| 00 |  |  |  |  |  |  |  |
| 01 |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 11 |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| (UD)Q2\Q1Q0 |  | 00 |  | 01 |  | 11 |  | 10 |
| 00 |  |  |  |  |  |  |  |  |
| 01 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 11 |  |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |

From the K-map we have, From the K-map we have,

*J*  (*UD*)*Q Q*  (*UD*)*Q Q*

2

1 0

 

1 0

*K*  (*UD*)*Q Q*  (*UD*)*Q Q*

2

1 0

 

1 0

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| (UD)Q2\Q1Q0 | 00 |  | 01 | 11 |  |  | 10 |
|  |  |  |  |  |  |  |  |
| 00 |  |  |  |  |  |  |  |
| 01 |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 11 |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| (UD)Q2\Q1Q0 | 00 |  | 01 | 11 |  |  | 10 |
| 00 |  |  |  |  |  |  |  |
| 01 |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| 11 |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |

From the K-map we have, From the K-map we have,

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | | x |  | |  | 1 |
| x |  |
| x |  | x |  | |  | 1 |
|  | |  | |
| x | | x | 1 |  |  | |
| x | | x | 1 |  |  | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | x | |  | x |
| 1 |
| 1 |  |  | x | |  | x |
|  | |  | |
|  | |  |  | | x | |
| 1 | x |  |
|  | | 1 | x |  | x | |
|  |  |

*J*  (*UD*)*Q*  (*UD*)*Q*

1

0



0

 (*UD*)  *Q*0 

*K*  (*UD*)*Q*  (*UD*)*Q*

1

0



0

 (*UD*)  *Q*0 

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| (UD)Q2\Q1Q0 | 00 | 01 | 11 | 10 |  |
|  |  |  |  |  |  |
| 00 | 1 | x | x | 1 |  |
| 01 | 1 | x | x | 1 |  |
| 11 | 1 | x | x | 1 |  |
| 10 | 1 | x | x | 1 |  |
|  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| (UD)Q2\Q1Q0 | 00 | 01 | 11 | 10 |  |
| 00 | x | 1 | 1 | x |  |
| 01 | x | 1 | 1 | x |  |
| 11 | x | 1 | 1 | x |  |
| 10 | x | 1 | 1 | x |  |
|  |  |  |  |  |  |

From the K-map we have, From the K-map we have,

*J*0  1

*K*0  1

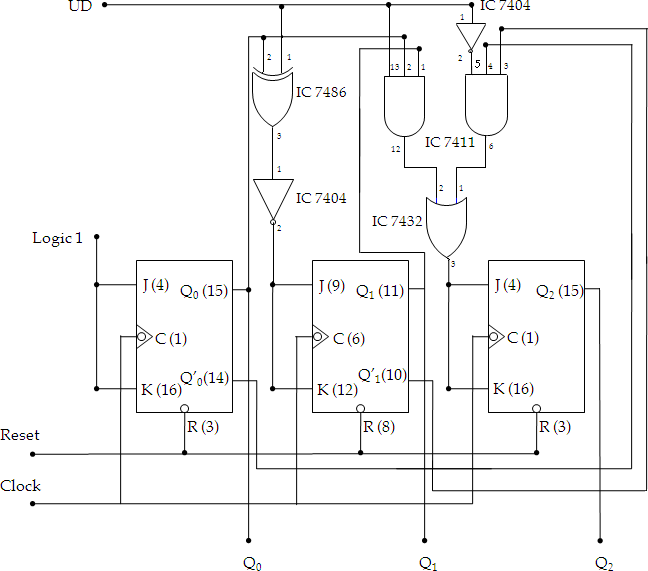


Figure. Connection diagram for Synchronous 3-bit Up/Down Counter using JK flip-flops

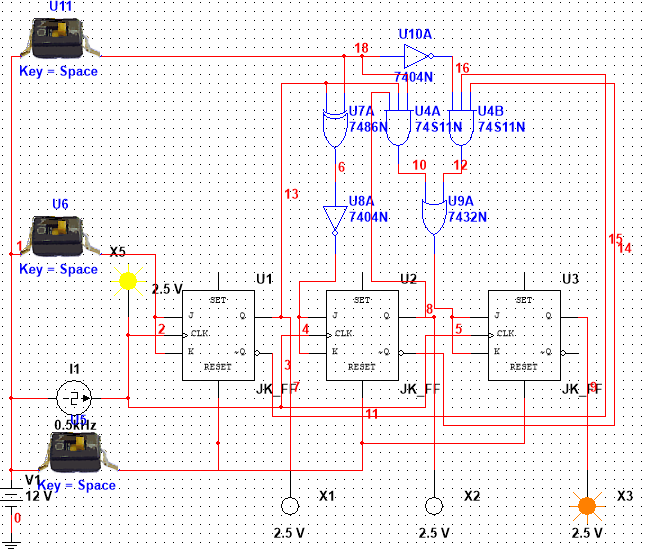


Figure:Multisim Circuit for 3-bit Synchronous Up/Down counter using JK flip-flops

**RESULT:**

A 3-bit Synchronous Up/Down Counter has been designed and implemented in MultiSim Software using JK flip-flops and has been verified using Truth Table.